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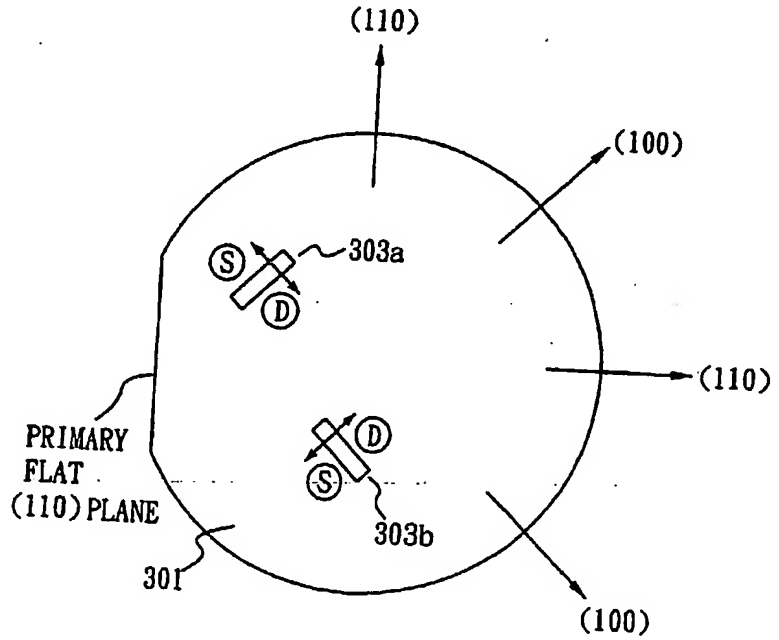
(54) Title: CMOS FABRICATION PROCESS UTILIZING SPECIAL TRANSISTOR ORIENTATION



(57) Abstract: Complementary metal oxide semiconductor transistors are formed on a silicon substrate. The substrate has a {100} crystallographic orientation. The transistors are formed on the substrate so that current flows in the channels of the transistors are parallel to the <100> direction. Additionally, longitudinal tensile stress is applied to the channels.

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patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

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INTERNATIONAL SEARCH REPORT

International Application No
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A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/8238 H01L27/092

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, PAJ, WPI Data, INSPEC, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 171 703 A (LIN YI-CHING ET AL) 15 December 1992 (1992-12-15) abstract; claims; figure 8 column 5, line 3 - line 8 column 9, line 48 - line 53 column 10, line 9 - line 11	1,2,6, 10,11
X	MATSUDA T ET AL: "ELECTRICAL CHARACTERISTICS OF 0ø/+-45ø/90ø-ORIEN TATION CMOSFET WITHSOURCE/DRAIN FABRICATED BY VARIOUS ION-IMPLANTATION METHODS" IEEE TRANSACTIONS ON ELECTRON DEVICES, IEEE INC. NEW YORK, US, vol. 46, no. 4, April 1999 (1999-04), pages 703-711, XP000906406 ISSN: 0018-9383 abstract; figure 1	1,2,6, 10,11

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
26 August 2002	30/08/2002

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax (+31-70) 340-3016	Wirner, C

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INTERNATIONAL SEARCH REPORT

International Application No
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
X	SAYAMA H ET AL: "EFFECT OF CHANNEL DIRECTION FOR HIGH PERFORMANCE SCE IMMUNE PMOSFET WITH LESS THAN 0.15MUM GATE LENGTH" INTERNATIONAL ELECTRON DEVICES MEETING 1999. IEDM. TECHNICAL DIGEST. WASHINGTON, DC, DEC. 5 - 8, 1999, NEW YORK, NY: IEEE, US, 1 August 2000 (2000-08-01), pages 657-660, XP000933266 ISBN: 0-7803-5411-7 the whole document	1,2,6, 10,11
Y		3-5,7-9, 12-15
Y	WELSER J ET AL: "Strain dependence of the performance enhancement in strained-Si n-MOSFETs" ELECTRON DEVICES MEETING, 1994. TECHNICAL DIGEST., INTERNATIONAL SAN FRANCISCO, CA, USA 11-14 DEC. 1994, NEW YORK, NY, USA,IEEE, 11 December 1994 (1994-12-11), pages 373-376, XP010131874 ISBN: 0-7803-2111-1 abstract; figure 1 page 373, left-hand column, paragraph 2	3,4,7,9, 12-14
Y	SCOTT G ET AL: "Effect of stress and dopant redistribution on trench-isolated narrow devices" CHALLENGES IN PROCESS INTEGRATION AND DEVICE TECHNOLOGY, SANTA CLARA, CA, USA, 18-19 SEPT. 2000, vol. 4181, pages 183-190, XP008006927 Proceedings of the SPIE - The International Society for Optical Engineering, 2000, SPIE-Int. Soc. Opt. Eng, USA ISSN: 0277-786X abstract; table 1 page 186, paragraph 3 -page 187, paragraph 1	5,8,15
A	EP 0 703 628 A (MOTOROLA INC) 27 March 1996 (1996-03-27) abstract; claims; figures	1,3,4,7, 9,10, 12-14

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International Application No
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	SCOTT G ET AL: "NMOS drive current reduction caused by transistor layout and trench isolation induced stress" ELECTRON DEVICES MEETING, 1999. IEDM TECHNICAL DIGEST. INTERNATIONAL WASHINGTON, DC, USA 5-8 DEC. 1999, PISCATAWAY, NJ, USA,IEEE, US, 5 December 1999 (1999-12-05), pages 827-830, XP010372197 ISBN: 0-7803-5410-9 abstract	1,5,7,8, 10,12-15
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